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PRIEST & GOLDSTEIN PLLC
5015 SOUTHPARK DRIVE
SUITE 230
DURHAM, NC 27713-7736

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,294	BARRY ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-19 have been presented for examination in this application. In response to the last office action, specification has been amended, drawing have been amended, claims 3,4,11,15 have been amended. As the result, claims 1-19 are now pending in this application.

Claims 1-19 are rejected.

Applicant's arguments filed 8/21/06 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained, with changes as needed to address the amendments.

Specification Objection

The abstract of the disclosure is objected to because it should not use phrase(s) which can be implied. In this instant the phrase "selectable means" is objected to.

Drawing

The drawing were received on 8/21/06. These drawings are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim 1 is rejected under 35 U.S.C. 102 (b) as being anticipated by Saulsbury et al (US 2002/0032710).

As in claim 1, Saulsbury describes a processor address translation apparatus for translating an instruction operand address to a different operand address (Saulsbury's Fig 6A, paragraph 20), the processor address translation apparatus comprising: a memory with an address input for selecting a data element from a plurality of data elements (Saulsbury's Fig 1: #32-1 dram); an instruction register for receiving an instruction encoded with an operand address and control information indicating the operand address is to be translated as part of the instruction's execution (Saulsbury's paragraphs 44,46 VLIW instructions load store; VLIW sub-instructions Fig 4) ; and an address translation unit for accessing the memory in a translation pattern, having the operand address as input and, in response to the instruction received in the instruction register, translating the operand address to form the different operand address in accordance with the translation pattern (Saulsbury's Fig 5 shows instructions translating operands rw,rx,ry,rz) , the different operand address accessing a data element from the memory through the address input (Saulsbury's paragraphs 24-25,35 describe distributed shared memory accessible by

processor's load store commands, the memory accessed by operand addresses of instruction as described in paragraph 44,lines 10-13).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al (US 2002/0032710) as applied to claim 1.

As in claim 2, Saulsbury describes wherein the address translation unit further comprises: a plurality of translation parameters and address translation functions supporting a plurality of translation patterns; and an input to select a translation pattern from the plurality of supported translation patterns. Saulsbury's page 6 paragraph 67 describes VLIW is configured to operate with multiple patterns of matrix transpose; Thus obviously, an input to the address translation circuits is required to indicate/select one of these different patterns for the processor and address translation circuits to operate on one of these patterns.

Claims 3-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al (US 2002/0032710) as applied to claim 2 and in view of Nair et al (US 6944747).

As in claim 3, the claim recites the processor address translation apparatus of claim 2 wherein the translation parameters include k by k s bits and k e bits for a k bit address and address translation functions further comprises combinatorial logic governed by the following equations; The claim further recites an equation to process matrix transpose of operand addresses. The claim's matrix transpose includes a function (e bits) to provide bit-wise invert of input operand address besides and, xor functions. Saulsbury does not describe the claim's detail of the matrix transpose. However, Nair describes an apparatus for matrix processing that can manipulate addresses bits using matrix multiply, addition, subtraction, bit-reverse operations etc..Nair teaches for these matrix operations, it is required the matrix transpose to have functions of bit-wises shifting, logical and, or, xor and bit inverting (i.e NOR, NAND) etc...(Nair's column 12, table 1) Thus it is obviously, the transpose matrix must includes the claim's e-bits vector since this vector merely providing the bit-wise invert function in the matrix transpose. It would have been obvious to one of ordinary skill in the art at the time of invention to include the matrix transposes as suggested by Nair in Saulsbury's system by storing the predetermined matrix transposes in a memory that is permanently or dynamically loaded into the system when needed; thereby providing the capability to quickly perform matrix operations.

As in claim 4, the claim recites wherein the instruction is a block load instruction. Saulsbury's paragraph 52 discloses a large matrix can be broken into multiple sub-matrices. Regardless of the matrix or sub matrices, Each of these matrices when executing the matrix transpose operation, provides the translation operand address for the first data element of the

matrix/sub-matrices and subsequent operand addresses for subsequent data elements in the matrix/sub-matrices. Thus the operation to access the transposed matrix/sub-matrices, that is the access can be a load or a store (see Saulsbury's paragraph 44 lines 8-12) requires the instruction/operation to operate on all addresses of data in these "blocks" matrix/sub-matrices.

As in claim 5, the claim recites the processor address translation apparatus of claim 1 disposed within a plurality of instruction operand address paths for a plurality of instructions, the plurality of instructions fetched for simultaneous execution (Saulsbury's paragraph 33 describes the VLIW sub-instructions are distributed to corresponding processing paths Fig 2: #56).

As in claim 6, Saulsbury describes wherein the plurality of instructions constitutes a very long instruction word VLIW (Saulsbury's paragraph 33).

As in claim 7, the rationale in the rejection of claims 1 and 2 is incorporated herein.The claim recites a processor register file indexing (RFM address translation apparatus for translating an RFI sequence of instruction operand addresses to an RFI sequence of different operand addresses, the processor RFI address translation apparatus comprising:

a memory with an address input for selecting a data element from a plurality of data elements (Saulsbury's Fig 1: #32-1)

an instruction register for receiving an instruction encoded with an operand address and control information indicating the operand address is to be translated as part of the instruction's execution (Saulsbury's Fig 3);

an RFI update unit enabled to generate on the RFI update unit's output a linear sequence of RFI operand addresses in response to a received sequence of RFI translation

type instructions (Saulsbury's paragraph 45,52 describes circuits required for decoding various instruction types, generates a sequence of source operands addresses for an VLIW sub-instruction; the destination operand addresses are used to update the register file for the next operation. The operation in block of matrix further requires a linear sequence of source and destination operand addresses specified in the sub-instructions).

A multiplexer for selecting between the operand addresses from the instruction Register for a first RFI operation and selecting the RWI update unit's output for subsequent RFI operations. (Salisbury's paragraphs 45,46 clearly describe the destination operand address/destination register of the current instructions are multiplexed and feedback to the source operand/source register for the subsequence instruction).

An address translation unit for accessing the memory in a translation pattern, receiving a sequence of operand addresses from the multiplexer and, in response to the sequence of RFI operand addresses, translating the sequence of RFI operand addresses to form a sequence of different operand addresses in accordance with the translation pattern, the different operand addresses each accessing a data element from the memory through the address input (Salisbury's paragraphs 51,52 describes the circuits for a matrix transpose operation on a block of operand addresses).

As in claim 8, the claim recites the processor RFI address translation apparatus of claim 7 disposed within PEs of an array of PEs. (Saulsbury's Fig 2, paragraph 34 describes circuits to process sub-instructions are correspond directly to each processing paths, Fig 2: #56. Thus each processing path that corresponds to the claim's PE contains address translation circuit for it's own register file, Fig 2: #60-1, #60-2).

As in claim 9, Saulsbury describes the processor RFI address translation apparatus of claim 7 disposed within a plurality of instruction operand address paths for a plurality of instructions, the plurality of instructions fetched for simultaneous execution. Saulsbury's paragraphs 34 describes using multiple processing paths that process instructions in a parallel manner help improve performance of the processing core.

Claim 10 rejected based on the same rationale as in the rejection of claim 6.

As in claim 11, the recites an address translation memory device for accessing data at translated addresses, the address translation memory device comprising: a first read address input, a storage device having data accessible at addressable locations, a second read address input internal to the address translation memory device for selecting data from the storage device during read operations, and a data output port;

The claim rejected based on the same rationale as of claim 1. Saulsbury discloses an address translation apparatus (Saulsbury's Fig 2: #50 instruction decode and issue logic) capable of translating an operand address of the instruction (corresponding to the claim's first read address input) to a transposed address (corresponding to the claimed second read address), internally to the address translation device (Saulsbury's Fig 2: #50), this transposed address selects data in the Register file, Saulsbury's Fig 2: #60-1 (corresponds to the claim's "selecting data from the storage device"), during the operation to access the data of the transposed matrix stored in register file. Saulsbury's paragraph 44 further discloses the access/operation comprises the load and/or store operations.

The claim further recites an address translation unit for accessing the storage device in a translation pattern, the address translation unit translating the first address input according with the translating pattern, to the storage device second read address input for reading data from the storage device at a translated address during the read operation.

The claim rejected based on the same rationale as discussed in above paragraphs. Saulsbury's Fig 6A clearly shows the first operand address is translated to the second operand address according to the matrix transpose pattern, to access the data of the transposed matrix stored in the register file Fig 2: #60-1.

As in claim 12, the claim rejected based on the same rationale as in the rejection of claim 11. Saulsbury's paragraph 44 further discloses the access/operation comprises the load and/or store operations.

As in claim 13, the claim recites wherein the storage device further comprises location selection logic merged with the address translation unit. The claim rejected based on the same rationale as in the rejection of claim 11. Saulsbury's Fig 2 shows the selection of registers in the register file Fig 2: #60-1 is implemented in the same "address translation unit", Fig 2: #50.

Claim 14 rejected based on the same rationale as in the rejection of claim 2.

Claim 15 rejected based on the same rationale as in the rejection of claim 3.

Claim 16 rejected based on the same rationale as in the rejection of claim 4.

Claim 17 rejected based on the same rationale as in the rejection of claim 3. It's obviously that matrix transpose operations AND,OR,XOR etc. as described by Nair must use combination logic.

Claim 18 rejected based on the same rationale as in the rejection of claims 1,3.

Claim 19 rejected based on the same rationale as in the rejection of claim 3.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

As to the remarks on pages 11-14 concerning the claim 1,

A) Regarding the remark "Saulsbury does not describe translating an instruction operand address to a different operand address", Examiner respectfully disagrees. Salibury discloses a VLIW processor having a matrix-transpose capability. The instruction to manipulate the matrix is shown in Salibury's Fig 4 with opcode bits 27:25 to indicate a matrix transpose instruction/command; source operand addresses (Fig 4: Rs2, Rs1 bits 17:6; paragraph 41 lines 1-2; paragraph 44 lines 8-13) to indicate the operand source addresses of the starting block/matrix (corresponding to the claim's "an instruction operand address") in which the matrix's data elements are stored the registers in the register file (Fig 2: #60, paragraph 34; corresponding to storing the data element of matrix in the memory of the claim). In response to the matrix transpose command/instruction, the subsequent source operand address value is transposed/translated into the corresponding destination operand address value (corresponding to the claim's translating.. to a different operand address) so that the data in the matrix stored in the register file is accessed/stored in a transposed manner (corresponding to the claim's using the translated/different address to access the "matrix" data element stored in the memory).

B) In regard to Applicant remark on page 13 lines 6-17 " trans0 ..specifies the source operands addresses.. which are not translated", and page 13 lines 18-19 "..the destination register

addresses are not translated. Examiner respectfully disagrees. As discussed in the item A, and shown in Saulsbury's Fig 6A, the corresponding destination addresses values are transposed/translated with respect to the source addresses values in order for the data in the matrix to be accessed in a transposed/translated manner. In other words, for the instruction/command that accesses the data of the matrix and in transposed mode, the source operand address value for data element "e" (i.e. address value is row 2, column 1, see Fig 600, Fig 500) will be transposed/translated to the destination operand address for data element "e" value of row 1, column 2, see Fig 600, Fig 502 in order to access the data "e" of the matrix and in transposed mode.

C) As to the remarks on page 14 concerning the claim 2 that states "..a plurality of translation parameters and address translation functions supporting a plurality of translation patterns". The language in the claim recites broadly translation patterns for an operation, wherein the operation can be understood as accessing data in the matrix in a transposed manner, and the translation patterns can be understood as translate/transpose the matrix based on using 2,4,8 or more multiple sub matrices patterns. Saulsbury's paragraph 52 discloses a method having such multiple sub matrices patterns in order to execute the "matrix transpose" operation faster, and in a concurrently manner.

D) Regarding the remarks on pages 15-16 for claims 3,4,7,16,18,
Nair's column 12 lines 13-20, table 1 discloses a mechanism including translation parameters as recited in claim 3 in order to further manipulate the address bits to achieve bit-wises shifting, logical and, or, xor, and bit inverting (i.e NOR, NAND). Thus the transpose matrix must have claim's 3 e-bits vector since this vector provides the bit-wise invert function in the matrix

transpose operation as taught by Nair. Applicant argues that Nair does not teach the "operand address" aspect. Examiner does not reply on Nair for expressly disclose of "operand address", because Saulsbury discloses this "operand address" aspect as discussed in items A and B.

Regarding the remark on page 15 for the amended claim 4 that recites, "wherein the instruction is a block load instruction". Saulsbury's paragraph 52 discloses a large matrix can be broken into multiple sub-matrices. Regardless of the matrix or sub matrices, Each of these matrices when executing the matrix transpose operation, provides the translation operand address for the first data element of the matrix/sub-matrices and subsequent operand addresses for subsequent data elements in the matrix/sub-matrices. Thus the operation to access the transposed matrix/sub-matrices, that is the access can be a load or a store (see Saulsbury's paragraph 44 lines 8-12) requires the instruction/operation to operate on all addresses of data in these "blocks" matrix/sub-matrices.

Regarding the remarks for claim 7, Examiner maintains the rejection as discussed in items A, B and C. Saulsbury clearly discloses the register file for a matrix translate/transpose operation as shown in Fig 2: #60, paragraph 45. Saulsbury's paragraph 52 discloses a large matrix can be broken into multiple sub-matrices. Regardless of the matrix or sub matrices, Each of these matrices when executing the matrix transpose operation, provides the translation operand address for the first data element of the matrix/sub-matrices and subsequent operand addresses for subsequent data elements in these matrix/sub-matrices.

Regarding the remarks for claim 16. The claim recites the limitations as of claims 1 and 4, that is translating/transposing the operand addresses in a "block" of matrix/matrices as discussed and rejected in above paragraphs.

Examiner maintains the rejection in claim 18 that recites similar limitation as of claims 1 and 3 and as discussed in items A-D above.

E) Regarding the remarks of claims 11-15 on pages 17-18, they are mooted in view of the amendments to the claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER

SERIAL NO.: 10/815,294
PETER H. PRIEST (919-806-1600)

Annotated Sheet Showing Changes

2/13

Approved
DD
10/19/06

FIG. 2A

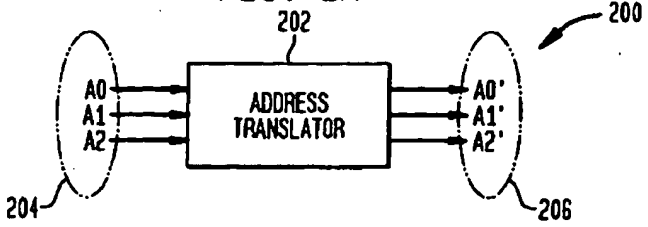

FIG. 2B

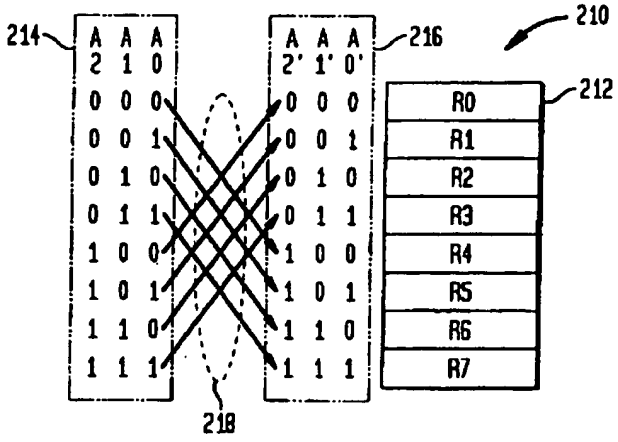

FIG. 2C